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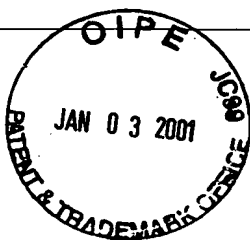
Docket No.: M4065.0340/P340
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Graham Kirsch

Serial No.: 09/652,003

Filed: August 31, 2000



Group Art Unit: 2185

Examiner: Not Yet Assigned

For: METHOD AND APPARATUS FOR
CONNECTING A MASSIVELY
PARALLEL PROCESSOR ARRAY TO A
MEMORY ARRAY IN A BIT SERIAL
MANNER

INFORMATION DISCLOSURE STATEMENT (IDS)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

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Technology Center 2100

Pursuant to 37 CFR 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned.

A copy of each reference on PTO/SB/08 is attached.


This Information Disclosure Statement is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR 1.97(g), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made. It is submitted that the Information Disclosure Statement is in compliance with 37 CFR 1.98 and the Examiner is respectfully requested to consider the listed references.

The Commissioner is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1073, under Order No. M4065.0340/P340. A duplicate copy of this paper is enclosed.

Dated: January 3, 2001

Respectfully submitted,

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